ASIC Verification Methodologies

- Directed Vs random
- Functional verification process
- Stimulus generation
- Bus functional model
- Monitors and reference models
- Coverage driven verification
- Verification planning and management

System Verilog Introduction

- Hardware Description Languages (HDLs)
- Flavors of System Verilog
- Language Basics Outline

Different Data Types

- Casting
- String
  - String Methods
- User defined Data types
  - Structure
  - Union
  - Enumeration
- Arrays
  - Packed
  - Unpacked
  - Fixed size array
  - Dynamic
  - Associative Array
  - Array Methods
- Queues
  - Queues Methods

Procedural Statement

- Conditional Statements
  - If else statements
  - Case statements
- Iteration Methods
  - For loop
  - While loop
  - Do while
  - Forever
  - Repeat
- Task and Function

Features of Verification

- Interface
- Clocking block
- Program block
- OOPs
  - Terminology
    - Class
    - Object
    - Handle
    - Properties
    - Method
  - Class routine
  - Inheritance
  - Polymorphism
  - Virtual Class
- Inter Process communication
  - Working with threads
  - Types of fork join
  - Semaphores
  - Mail box
- Randomization
  - Randomization function
  - Types of randomization
  - Random Constraints
  - Constraints block
- Assertions
  - Concurrent assertions
  - Immediate assertions
  - Property block
  - Sequence block
  - Assert, assume and cover
- Coverage
  - Coverage type
  - Coverage strategy
  - Coverage model
  - Coverage points.
  - Cross coverage