

INTRODUCTION TO VLSI

- Need, Scope, Use and History of VLSI
- Introduction to Chip Design Process
- Description of Hardware Description Languages
- Applications of VLSI
- Evolution of Computer Aided Digital Design
- Emergence of HDL's
- VLSI Design Flow.
- Importance of HDL's.

INTRODUCTION TO VERILOG HDL

- Need, Scope, Use and History of Verilog HDL
- Special Features of Verilog HDL
- Application of Verilog HDL in Market and Industries
- Discussion of Verilog HDL & other procedural language.

DESIGNING IN VERILOG HDL

- Design Methodology
 - Top-Down Methodology
 - Bottom-up Methodology
- Design Simulation and Design Synthesis
- Verilog HDL Design Flow
- Keyword description in VERILOG HDL
 - Module Description

DATA TYPES IN VERILOG HDL

- Lexical Conventions
- Description of Data types
 - Net
 - Register
- Scalar Data Description
- Vector Data Description
- Parameters Description
- Array Description

INTRODUCTION OF DIFFERENT MODELING STYLE

- Gate level Modeling
- Dataflow modeling
- Behavioral Modeling
- Switch level Modeling

GATE LEVEL MODELING

- Logic Gate Primitive
- Gate Instantiation
- Design RTL from Logic Diagram
- Delays in Gate-Level Design
 - Rise Delay
 - Fall Delay
 - Turn off Delay

DATAFLOW MODELING

- Continuous Assignment statement
- Implicit Assignment statement
- Delay
 - Assignment Delay
 - Implicit Assignment Delay
 - Net declaration Delay
- Expressions
- Basic operators
- Verilog specific operators(case equality etc)
- Operands
- Operator Precedence

BEHAVIORAL MODELING

- Structured Procedural Statements
 - Always Statements
 - Initial Statements
- Blocking Statement
- Non blocking Statement
- Timing Control Statement
 - Delay Based Timing Control
 - Event Based Timing Control
- Conditional statements
 - If-else statements
 - Case statements
- Loops
 - While loop
 - For loop
 - Repeat loop
 - Forever loop
- Block Statements
 - Parallel block
 - Sequential block

FINITE STATE MACHINE (FSM)

- Introduction to FSM

- Mealy Machine
- Moore Machine
- Flip-flops
- Counters

MINOR PROJECTS

- TLC by Sensors
- TLC four way based on timing control
- ALU Design
- Shift unit Design
 - LFSR (Linear feedback shift register)
 - MISR (Multiple input signature register)
- Booth multiplier
- Wallace multiplier
- Comparator unit design

HARDWARE IMPLEMENTATION

- Introduction to FPGA
- Introduction to CPLD
- Brief discussion of Hardware kit
- Working on Physical FPGA and CPLD
- Led interfacing.
- 7-segment interfacing.
- LCD interfacing.
- Keypad scanner.
- Clock divider RTL code

USEFUL MODELING TECHNIQUE

- Procedural Continuous Assignment Statement
 - Assign Statement
 - Deassign Statement
 - Force Statement
 - Release Statement
- Defparam Statement
- Switch level Modeling style
 - MOS Switches
 - Bidirectional Pass Switches.
 - Resistive MOS Switches
- Introduction to system Verilog
- Sub programs
- Tasks
- Functions
- Difference between Tasks and Functions
- Understanding of Automatic keyword in Tasks and Functions

- User Defined Primitives (UDP's)
 - Combinational UDP'S
 - Sequential UDP'S.
- Verilog Test bench
- Test Bench for Combinational Design
- Test Bench for Sequential Design
- Sequential block(Begin-End)
- Parallel Block(Fork-Join)
- Logic synthesis
- System Task
 - \$display
 - \$monitor
 - \$finish
 - \$stop
 - \$random
- Compiler Directives
 - `define
 - `include
 - `ifdef
 - `ifndef
 - `timescale

MEMORY MODELING

- RAM & ROM designing
- Bi - directional ports
- Case X and Case Z statements

MAJOR PROJECTS

- Assistance on any project brought by student.
- Universal asynchronous receiving and transmitting